UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/026,790	02/20/98	DUPENLOUP	G 30454-122(P-

LM02/0819

MITCHELL SILBERBERG & KNUPP
11377 WEST OLYMPIC BOULEVARD
LOS ANGELES CA 90064-1683

EXAMINER	
THOMPSON, A	
ART UNIT	**PAPER NUMBER**
2763	4

DATE MAILED: 08/19/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/026,790	Applicant(s) Guy DUPENLOUP
	Examiner A.M. Thompson	Group Art Unit 2763

☒ Responsive to communication(s) filed on *Feb 20, 1998* .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-14* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-14* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

This Application, number 09/026790, has been examined. Claims 1-14 are pending.

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because applicant uses patent claim phraseology. Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities: Page 16 requires the following changes: line 2, "extend" changed to *extent*; line 22, "at" changed to *out*; lines 5, 25, "multiply" changed to *multiple*. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Gupte et al. (hereinafter "Gupte"), U.S. Patent No. 5,812,416. Gupte discloses a computer-aided system and method for design, verification, implementation, and signoff of ASICs. Column 1, ll. 62-65.

Pursuant to Claim 1, Gupte discloses "a method of generating synthesis scripts to synthesize integrated circuit (IC) designs from a generic netlist description into gate-level description": column 3, ll. 8-10, ll. 22-34; see also Claim 1. Gupte's method comprises the steps of :

identifying hardware elements in the generic netlist: Parsing inherently involves the identification of hardware elements in the HDL code (generic netlist), column 14, ll. 12-17;

determining key pins for each of said identified hardware elements: Parsing inherently involves determining key pins for identified hardware elements;

extracting design structure and hierarchy from the Generic netlist: column 14, ll. 12-22;

generating script to cause a logic synthesis tool to apply bottom-up synthesis to modules and sub-modules of the IC design: column 14, ll. 32-35, ll. 39-48;

generating script to cause a logic synthesis tool to apply top-down characterization to modules and sub-modules of the IC design: column 14, ll. 49-52; and

generating script to cause a logic synthesis tool to repeat said bottom-up and said top-down applications until constraints are satisfied: See Figure 14 which illustrates the top-down and bottom up synthesization process, and especially step 812, which emphasizes that these processes may be repeated. Also see, column 14, ll. 52-55.

Pursuant to Claim 2, Gupte's "step of extracting design structure allows for a multilevel structuring of modules of the IC design": Various commands may be used that impact a design's hierarchy, see column 14, line 65 to column 16, line 24.

Pursuant to Claim 3, Gupte also discloses "the step of generating script to cause a logic synthesis tool to apply initial mapping to the IC design": see Figure 12, also note column 13, ll. 10-49; In initial mapping default constraints are used: column 14, ll. 39-41. Also see Fig. 14, step 800.

Pursuant to Claim 4, "wherein the logic synthesis tool is Synopsys Design Compiler": An embodiment of the Gupte invention uses the Synopsis Design Compiler, column 7, ll. 6-19.

Pursuant to Claim 5, "further comprising the step of rearranging design hierarchy by changing the design": Gupte teaches that incremental changes to design modules may result in hierarchical changes. Column 3, ll. 8-21.

Pursuant to Claim 6, "further comprising the step of generating script to cause a logic synthesis tool to ungroup modules of the IC design": Gupte teaches a method in which a recipe file is processed during script generation that performs an UNGROUP procedure. See Figs. 15B and 15C. See also, column 14, ll. 65-67, column 15, ll. 43-67, column 16, ll. 1-24.

Pursuant to Claim 7, Gupte also discloses a synthesis script generation tool: Gupte teaches a synthesis script generation tool, see Gupte's Fig. 12, step 700, also see column 13, ll. 24-61; comprising

extractor to extract synthesis-related design information from a file having the design information: column 14, ll. 12-22;

target technology library to provide technology cells and hardware : In Gupte, the HDL code and constraints are input to the Synthesis Script Generation Tool (see Figure 12), and Gupte teaches and claims that these constraints include technology information, column 20, Claim 9;

script generator for a logic synthesis tool: Gupte's Fig. 12 shows that the output of the script generator, illustrated by Fig. 12, step 712, is input to a logic synthesis tool, Fig. 12, step 714.

Pursuant to Claim 8, "wherein the logic synthesis tool is Synopsys Design Compiler": Gupte discloses that a preferred embodiment of a synthesis tool comes from Synopsis, column 13, ll. 62-64;

Pursuant to Claim 9, "an apparatus for generating synthesis scripts . . . comprising a processor . . .": Gupte discloses a computer system that executes software which includes a script generator. Column 5, line 58 to column 6, line 28. See also Figs. 1, 2; comprising

a processor: See Gupte's Fig. 2, block 102, also see column 6, ll. 9-17;

memory connected to said processor: see Gupte's Fig. 2, block 104, see also column 6, ll. 9-17;

said memory having instructions for said processor: Gupte teaches that computer programs that implement the invention are stored in memory, column 5, ll. 58-67;

to determine key pins . . .: Parsing inherently involves determining key pins for identified hardware elements;

extract critical design structure and hierarchy from the generic netlist: column 14, ll. 12-22;

apply bottom-up synthesis to modules and sub-modules: column 14, ll. 32-35, ll. 39-48;

apply top-down characterization to modules and sub-modules . . .: column 14, ll. 49-52;

repeat said bottom-up and said top-down applications . . .: See Figure 14 which illustrates the top-down and bottom up synthesization process, and especially step 812, which emphasizes that these processes may be repeated. Also see, column 14, ll. 52-55.

create design compile scripts to synthesize modules and sub-modules . . .: see column 14, ll. 39-55.

Pursuant to Claim 10, "an apparatus for generating synthesis scripts to synthesize integrated circuit (IC) designs. . ." : Gupte discloses a computer system that executes software that includes script generation code; Column 5, line 58 to column 6, line 28. See also Figs. 1, 2; comprising

means for determining key pins. . .: Parsing inherently involves determining key pins for identified hardware elements;

means for extracting critical design structure and hierarchy . . .: column 14, ll. 12-22;

means for applying bottom-up synthesis to modules and sub-modules. . .: column 14, ll. 32-35, ll. 39-48;

means for applying top-down characterization to modules and sub-modules . . .: column 14, ll. 49-52;

means for repeating said bottom-up and said top-down applications: See Figure 14 which illustrates the top-down and bottom up synthesization process, and especially step 812, which emphasizes that these processes may be repeated. Also see, column 14, ll. 52-55;

means for creating design compile scripts to synthesize modules. . .: see column 14, ll. 39-55.

Pursuant to Claim 11, " a computer storage medium containing instructions for generating synthesis scripts": See Figure 1's illustration of a computer system for implementing Gupte's invention. Gupte discloses a floppy disk utilized to store and retrieve program code that implements the Gupte invention, column 5, line 58 to column 6, line 5;

identifying hardware elements in the generic netlist . . .: Parsing inherently involves the identification of hardware elements in the HDL code (generic netlist), column 14, ll. 12-17;

determining key pins for each of said identified hardware elements: Parsing inherently involves determining key pins for identified hardware elements;

extracting critical design structure and hierarchy from the generic netlist: column 14, ll. 12-22;

applying bottom-up synthesis to modules and sub-modules: column 14, ll. 32-35, ll. 39-48;

applying top-down characterization to modules and sub-modules: column 14, ll. 49-52;

repeating said bottom-up and said top-down applications: See Figure 14 which illustrates the top-down and bottom up synthesization process, and especially step 812, which emphasizes that these processes may be repeated. Also see, column 14, ll. 52-55;

creating design compile scripts to synthesize modules: see column 14, ll. 39-55.

Pursuant to Claim 12, "wherein said computer storage medium is selected from a group consisting of magnetic device, optical device. . .": Gupte's invention teaches the use of other computer-readable media in addition to a floppy disk, column 5, line 63 to column 6, line 2.

Pursuant to Claim 13, "a process for generating synthesis scripts . . .": Gupte teaches a method for automatically generating synthesis scripts, see Gupte's Fig. 13, 14, also see column 14, ll. 4-48; comprising the steps of

identifying hardware elements in the generic netlist: Parsing inherently involves the identification of hardware elements in the HDL code (generic netlist), column 14, ll. 12-17;

determining key pins for each of said identified hardware elements: Parsing inherently involves determining key pins for identified hardware elements;

extracting critical design structure and hierarchy from the generic netlist: column 14, ll. 12-22;

applying bottom-up synthesis to modules and sub-modules: column 14, ll. 32-35, ll. 39-48;

applying top-down characterization to modules and sub-modules: column 14, ll. 49-52;

repeating said bottom-up and said top-down applications: See Figure 14 which illustrates the top-down and bottom up synthesization process, and especially step 812, which emphasizes that these processes may be repeated. Also see, column 14, ll. 52-55;

creating design compile scripts to synthesize modules: see column 14, ll. 39-55.

Pursuant to Claim 14, a computer system for generating synthesis scripts. . .": Gupte discloses a computer system that executes the synthesis script generation software, column 13, ll. 10-67 to column 14, ll. 1-3;

means for determining key pins. . .: Parsing inherently involves determining key pins for identified hardware elements;

means for extracting critical design structure and hierarchy . . .: column 14, ll. 12-22;

means for applying bottom-up synthesis to modules and sub-modules. . .: column 14, ll. 32-35, ll. 39-48;

means for applying top-down characterization to modules and sub-modules . . .: column 14, ll. 49-52;

means for repeating said bottom-up and said top-down applications: See Figure 14 which illustrates the top-down and bottom up synthesization process, and especially step 812, which emphasizes that these processes may be repeated. Also see, column 14, ll. 52-55;

means for creating design compile scripts to synthesize modules. . .: see column 14, ll. 39-55.

Claim Rejections - 35 USC § 103

7. Claim 7 is also rejected under 35 U.S.C. 103(a) as being unpatentable over Gupte. Gupte discloses a computer-aided system and method for design, verification, implementation, and signoff of ASICs. Column 1, ll. 62-65.

Gupte discloses a synthesis script generation tool: Gupte teaches a synthesis script generation tool, see Gupte's Fig. 12, step 700, also see column 13, ll. 25-61; comprising

extractor to extract synthesis-related design information from a file having the design information: column 14, ll. 12-22;

target technology library to provide technology cells and hardware characteristics of the cells for mapping purposes: In Gupte, the HDL code and constraints are input to the Synthesis Script Generation Tool (see Figure 12) and Gupte teaches and claims that these constraints include technology information, column 20, Claim 9.

Gupte's Fig. 12 show the technology library, Fig. 12, step 716, as input to the synthesis tool, Fig. 12, step 714. Examiner interprets this as illustrative of the logic synthesis process shown in Applicant's Figure 36 and not an indication that Gupte's design specific synthesis scripts, Fig. 12, step 712, lack technology specificity. But even if applicant asserts that step 712 is not technology specific, it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify Gupte and input the technology library information to the synthesis script generation tool to produce a technology specific (technology dependent) synthesis script for effective and efficient design mapping;

script generator for a logic synthesis tool: Gupte's Fig. 12 shows that the output of the script generator, Fig. 12, step 712, is input into a logic synthesis tool, Fig. 12, step 714.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

▹ Rostoker et al., U.S. Patent No. 5,572,437, discloses an automatic logic-model generation system.

▷ Rostoker et al., U.S. Patent No. 5,544,067, teaches a system for interactive design, synthesis and simulation of an electronic system allowing a user to design a system either by specification or by graphical entry.

▷ Rostoker et al., U.S. Patent No. 5,557,531, discloses a methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications.

▷ Dangelo et al., U.S. Patent No. 5,880,971, discloses a methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications.

▷ Gupte et al, U.S. Patent No. 5,903,475, teaches a system and method of verifying the design of an ASIC during design and implementation.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The examiner can normally be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900 or the Customer Service Center whose telephone number is (703) 306-5631.

AMT
AUGUST 9, 1999

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER